Enter
TP
5/2/06

Clean Version

SUBSTITUTE SPECIFICATION

SEMICONDUCTOR DEVICE

CROSS-REFERENCE TO RELATED APPLICATION

The present application claims priority from Japanese patent application JP 2003-108604 filed on April 14, 2003, the content of which is hereby incorporated by reference into this application.

BACKGROUND OF THE INVENTION

The present invention relates to a nonvolatile memory enabling electric erase and write and to a semiconductor integrated circuit such as a data processor called a microcomputer or a microprocessor equipped with the nonvolatile memory together with a central processing unit (also called a CPU), e.g., to a technique effective to be applied to a microcomputer equipped with a flash memory.

In the read operation of a flash memory, 1) a read bit line is precharged, 2) a word line is started up at a selective level such as a high level ("H") to turn on a memory cell transistor, 3) upon flowing of a memory current via the memory cell transistor, the precharged bit line is drawn out to a low level ("L"), and 4) the potential of the bit line drawn out to the low level is sensed by a sense amp.

When a threshold voltage (Vth) of a memory cell transistor is lower than a word line potential (word line selected level),